**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently amended) A method for observing the state of internal signals during chip testing, comprising:

receiving specific test signals by a plurality of multiplexers in at least one module;

combining, by the plurality of multiplexers, test signals received for each test signal group to create a plurality of test signal groups;

receiving, by mapping logic, one of said plurality of test signal groups from each one of said plurality of multiplexers; and

~~mapping, by said mapping logic, one of said plurality of test signal groups to any one of a plurality of outputs of said mapping logic to output as a test output group.~~

mapping, by said mapping logic, one of said plurality of test signal groups to at least two of said plurality of outputs of said mapping logic concurrently to output as two different test output groups.

2. (Original) The method of claim 1 wherein the at least one module includes a plurality of modules.

3. (Original) The method of claim 2, further comprising:

concurrently observing test signals for a plurality of modules.

4. (Original) The method of claim 3 wherein the plurality of modules includes identical modules.

5. (Previously presented) The method of claim 1 further comprising:

said mapping logic including a plurality of mapping multiplexers;

each one of said plurality of mapping multiplexers receiving said plurality of test signal groups;

each one of said plurality of mapping multiplexers generating a different one of said plurality of outputs of said mapping logic; and

each one of said plurality of mapping multiplexers selecting one of said plurality of test signal groups to output as a test output group.

6. (Previously presented) The method of claim 1 wherein said mapping logic is byte lane mapping logic.

7. (Canceled)

8. (Currently amended) A system for observing the state of internal signals during chip testing, comprising:

means for receiving specific test signals by a plurality of multiplexers in at least one module;

the plurality of multiplexers combining the specific test signals received for each test signal group to create a plurality of test signal groups;

mapping logic for receiving one of said plurality of test signal groups from each one of said plurality of multiplexers; and

~~said mapping logic mapping one of said plurality of test signal groups to any one of a plurality of outputs of said mapping logic to output as a test output group~~.

said mapping logic mapping one of said plurality of test signal groups to at least two of said plurality of outputs of said mapping logic concurrently to output as two different test output groups.

9. (Original) The system of claim 8 wherein the at least one module includes a plurality of modules.

10. (Original) The system of claim 9, further comprising:

concurrently observing test signals for a plurality of modules.

11. (Original) The system of claim 10 wherein the plurality of modules includes identical modules.

12. (Previously presented) The system of claim 8 further comprising:

said mapping logic including a plurality of mapping multiplexers;

each one of said plurality of mapping multiplexers receiving said plurality of test signal groups;

each one of said plurality of mapping multiplexers generating a different one of said plurality of outputs of said mapping logic; and

each one of said plurality of mapping multiplexers selecting one of said plurality of test signal groups to output as a test output group.

13. (Previously presented) The system of claim 8 wherein the mapping logic is byte lane mapping logic.

14. (Previously presented) The method according to claim 1, further comprising:

mapping, by said mapping logic, a first one of said plurality of test signal groups, which was received from a first one of said plurality of multiplexers, to a first one of said plurality of outputs of said mapping logic to output as a first test output group;

mapping, by said mapping logic, a second one of said plurality of test signal groups, which was received from a second one of said plurality of multiplexers, to a second one of said plurality of outputs of said mapping logic to output as a second test output group; and

said first one of said plurality of test signal groups and said second one of said plurality of test signal groups being a same signal type of signal.

15. (Previously presented) The system according to claim 8, further comprising:

said mapping logic mapping a first one of said plurality of test signal groups, which was received from a first one of said plurality of multiplexers, to a first one of said plurality of outputs of said mapping logic to output as a first test output group;

said mapping logic mapping a second one of said plurality of test signal groups, which was received from a second one of said plurality of multiplexers, to a second one of said plurality of outputs of said mapping logic to output as a second test output group; and

said first one of said plurality of test signal groups and said second one of said plurality of test signal groups being a same signal type of signal.